Inspection of lead-free advanced packages: flip chip and chip-scale under control

Verification method for high challenges

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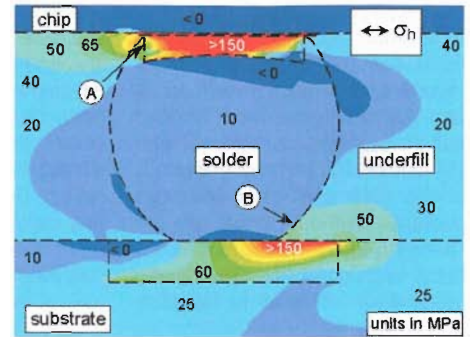

Figure 3: Cell analysis – possible failure interface red color indicates maximum stress area

Lead-free implementation presents the next challenges for board assemblers from a design, soldering process, and QC/QA (quality control and assurance) view. The higher reflow temperatures will cause greater thermal stress to PCBs and components. The smaller process window will make the soldering task more difficult, placed between the lead-free alloy melting point and the maximum allowable component temperature. Challenges have to be considered to guarantee required DPM (defects per million) levels and a minimum of in-field failures. In particular, the very small solder joints found on flip-chip (FC) and chip-scale packages (CSP) will see a great deal more thermal stress during soldering which can result in fatal defects.

Especially a large issue in these cases is the topside ball delamination for the area-array packages FC and CSP. Recent research shows important failure-analysis data relating to FC and CSP reliability in both tin-lead and lead-free soldering processes. A new optical inspection technology designed to detect such defects in a non-destructive manner is a viable tool for inspecting and detecting those defects. The internal designs of FCs and CSPs vary greatly from manufacturer to manufacturer. Two internal designs can be seen in figures 1 and 2.

In any case, the extremely small component side joints of an FC or CSP are at greater risk of failing under mechanical stress. Toshio Nakamura and Gary Yu Gu have conducted extensive research aimed at understanding the failure mechanism by identifying likely fracture modes and potential delamination sites in flip-chip packages. Their research, entitled Mechanical Behaviors of Flip-Chip Packaging, shows that the upper solder connection is at greater risk of delamination as seen in figure 3.

In the publication Mechanical Reliability of Underfilled CSP Assemblies by Murtuza Rampurawala, the authors Michael Meilunas, Arun Gowda and K. Srihari call attention to the problem of topside ball delamination of CSP joints: Cross-sectional analysis of failed assemblies found cracks within the solder joint along the component side of the assembly. Figure 4 shows an image of a non-underfilled sample of a package that failed in torsional testing. The crack initiated from the interface of the solder mask and the pad of the component. Figure 5 shows a cross-section of an underfilled package which failed after 1825 torsion cycles.

Underfill is used for FCs and some CSPs in order to mechanically strengthen the joint after soldering. If delamination occurs before the underfill process and is not detected, this will cause an early in-field failure. Many area-array packages including CSPs are positioned on an interposer which compensates for the internal tension in a solder joint which is created by high CTE (coefficient of thermal expansion) mismatch during the heating and cooling process. The general problem with CTE mismatch is illustrated in figure 6. Due to the fact that the CTE from the substrate and the component body are not the same, there is a relative movement differential between the expanding materials which increases at higher process temperatures. During cooling there is a relative movement differential between the contracting materials which can cause a shearing.

Figure 7 addresses the fact that this movement is greater at the corners of the component. Considering the component from the center outwards, the relative movement at the center ball is zero. As we move towards the corners of the package, the relative movement differential increases as the distance from the center point increases. The differential is greater at solder ball 6 (ΔX_6), for example, than at solder ball 3 (ΔX_3). During cooling the materials contract and the relative movement between the

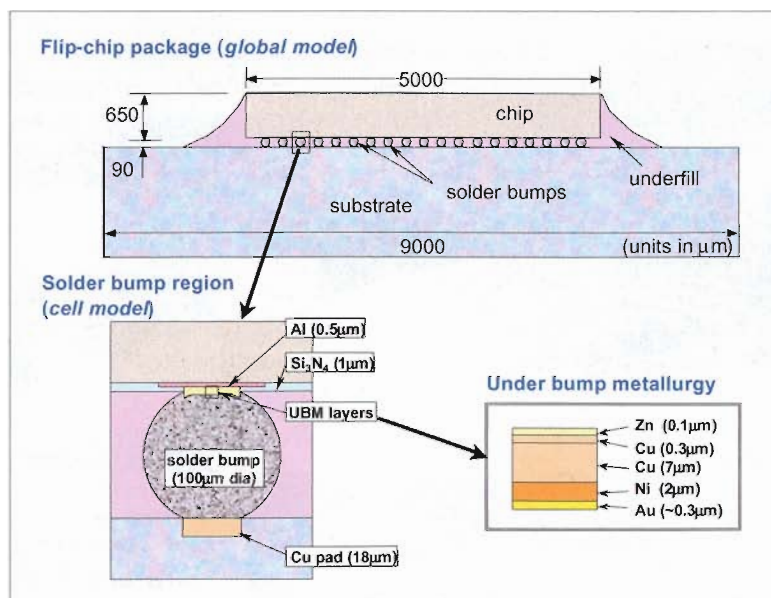

Figure 1: Example of a flip-chip solder bump and its different materials and layers

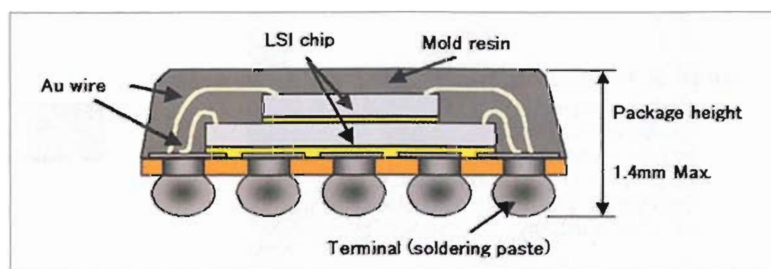

Figure 2: A typical chip-scale package (CSP) and its design

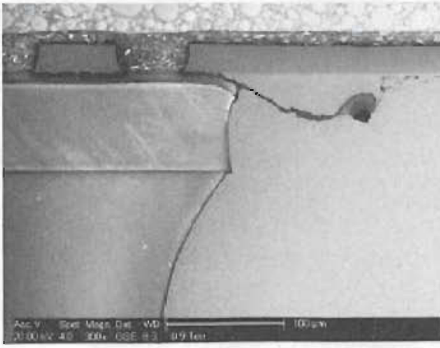

Figure 4: Non-underfilled package that failed in torsional testing

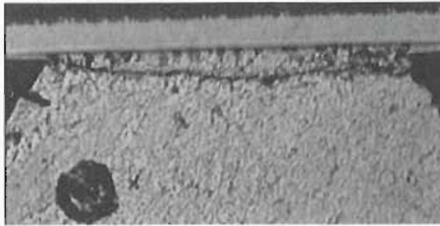

Figure 5: Cross-section of underfilled package which failed after 1825 cycles

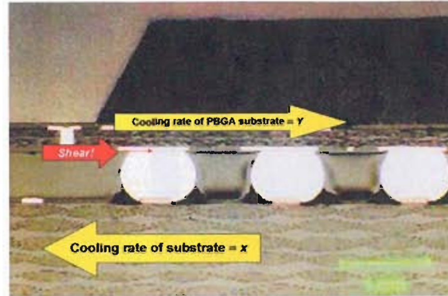

Figure 6: Cross section of BGA revealing shearing zone, caused by CTE mismatch during cooling

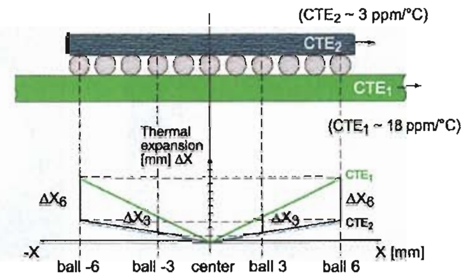

Figure 7: The corner balls are at greater risk of delamination caused by CTE mismatch

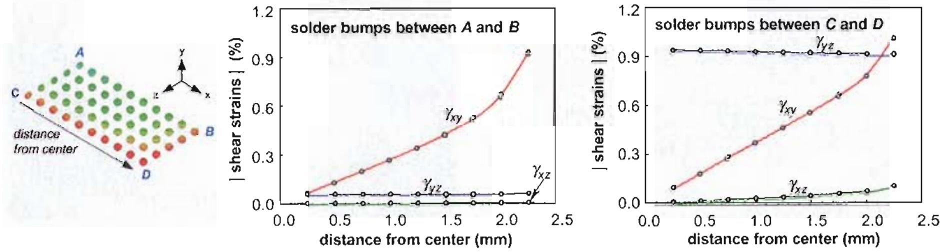

Figure 8: Increased shear strain at corner solder balls

PCB and the component is impeded by the solidification of the solder. As all materials will assume their original position at room temperature, a residual sheer stress will remain in the solder joint. This stress is substantially larger at the corners of the component and can result in micro-crack formation. For this reason, it is essential that PCB-design engineers choose the right material combinations with respect to their CTE mismatch.

In their research entitled 3D Interfacial Delamination Near Solder Bumps in Flip-Chip Package, the authors Yu Gu and Toshio Nakamura underscore this issue of increased stress at the corners of the package. Figure 8 reveals that there is increasing shear strain from the center to the edge, and that out-of-plane shear strain is larger near the edges of the component.

How does solder-joint failure increase?

This analysis of the problems of increased corner-ball stress as it relates to area-array packages, especially in a lead-free process, is highlighted in a publication entitled HDPUG's Failure Analysis of High-Density Packages' Lead-Free Solder Joints: It can be seen that due to the higher lead-free reflow temperatures, the package is warped severely, leading to the anomalous-shape solder joints near the corner, and fatter than normal shape joints near the middle. The failure locations of the solder joints of the package are near the corners of the outer, inner and the thermal ball arrays. This is due to the global thermal-expansion mismatch between the package (silicon chip, molding compound), and BT (bismaleimide triazene) substrate and the PCB, and the local thermal-expansion mismatch between the silicon chip, the BT substrate, and the molding compound.

The basic problems associated with FC and CSP solder joints as discussed are amplified in a lead-free process due to three essential factors:

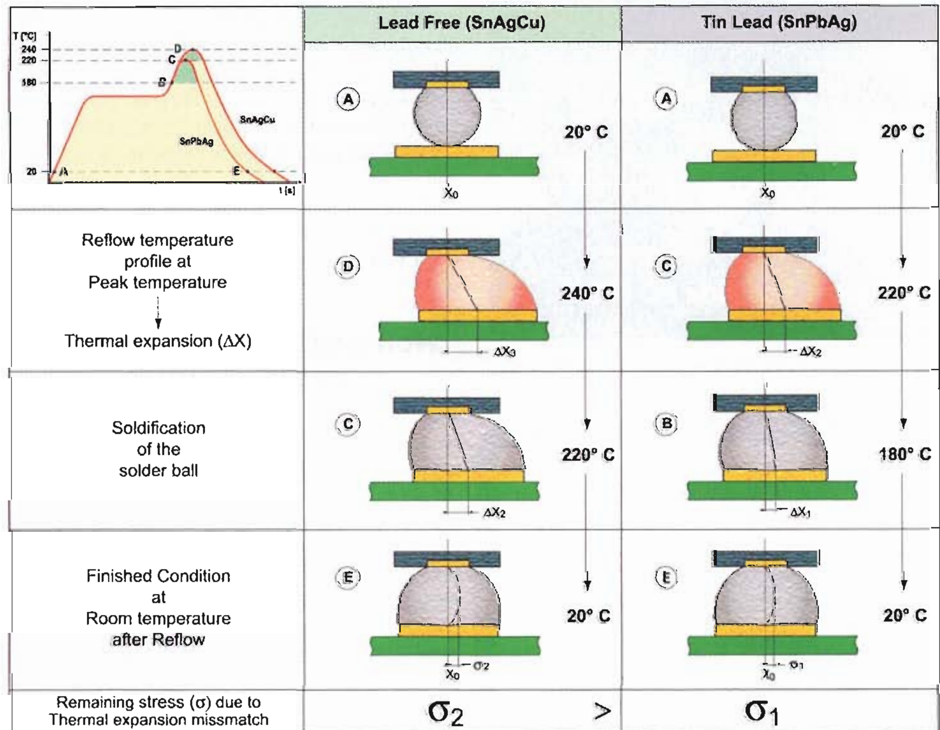

Figure 9: Cooling behavior between lead-free (left) and lead-containing (right) solder balls

- The process temperatures for lead free is higher
- The temperature that a lead-free solder joint solidifies is much higher and closer to the peak-reflow temperature than with SnPb
- The effects of CTE mismatch are amplified at higher temperatures

The start up condition in both processes is the same at room temperature – figure 9 identifies the problems in more detail (point A). As the assembly heats up in a reflow process, the relative expansion differential (ΔX_3) in a lead-free process is greater at the higher peak temperature (D) than the relative expansion (ΔX_2) in a tin-lead process at its peak (C). At position (C) in the temperature profile, the lead free alloy solidifies at position ΔX_2, whereas the tin-lead alloy is at its peak temperature. Therefore, during cooling, the contraction of the materials in the tin-lead process takes place longer in a fluid or flexible state, and can move back to position (ΔX_1) at the ball-solidification point (B). When all materials move back to their original positions (X_0) at room temperature (E), the remaining stress

Figure 10: Cracked solder joints for SnPb and SnAgCu alloys due to temperature cycling

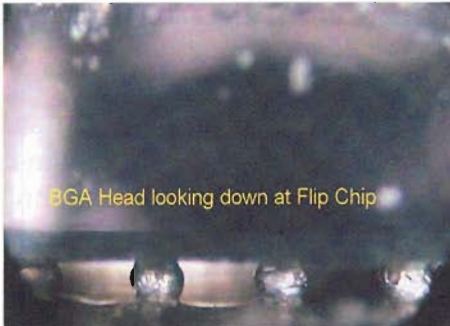

Figure 11: Standard BGA optics looks down at bottom fillet

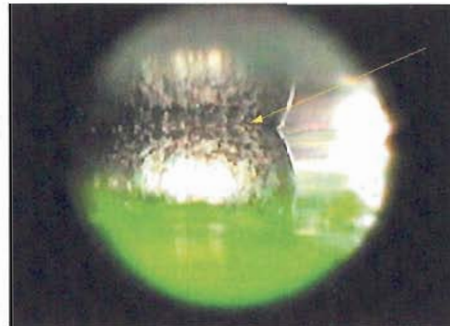

Figure 13: Corner ball of BGA delaminated

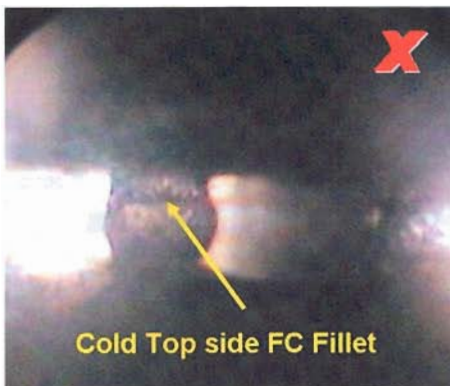

Figure 12: New FC optics look up at topside fillet

(σ2) in the lead free-solder joint is greater than (σ1) in the tin-lead joint. It should be understood that the remaining stress (σ) can result in a shearing or delamination even during the first production reflow cycle. Proper inspection techniques should allow for the detection and correction of such defects before they become costly in-field failures.

In the paper, Reliability of Lead-Free Solder Connections for Area-Array Packages by Ahmer Syed, Amkor Technology, the author underscores the top side delamination problem as it relates to the lead-free process: The failures reported were analyzed with dye and pry and cross-sectioning techniques. Overall, it was found that solder joint failure for all of these Pb-free alloys occur at the package side of the joint as is the case for SnPb alloy. A representative cross-section of joints with SnPb and SnAgCu alloys is shown in Figure 10. In another publication, Accumulated Creep Strain and Energy Density Based Thermal Fatigue Life Prediction Models for SnAgCu Solder Joints, Ahmer Syed further underscored this problem: In all cases reported, the (SAC alloy, editorial note) solder joints failed at package interface.

For the CTE-mismatch issue, and considering the fact that corner joints of an area-array package have greater stress, it is clear that the lead-free process for FCs and CSPs will realize a much greater danger for topside ball delamination. The excerpts from the research highlighted in the articles noted above underscore the problems associated with component-side delamination on a variety of FC and CSP devices. Greater care must be taken, therefore, during both the PCB design and production phases in order to minimize this problem. Most importantly, however, first article inspection procedures must be implemented in order to discover these fatal errors before they end up as costly in-field failures.

Non-destructive detection of the defects

Area-array packages in general and FC and CSP packages in particular have presented great challenges for inspection equipment. The problem lies simply in the fact that the solder connections are both extremely small and are hidden under the package. The cross sectioning of such devices is a timely and costly undertaking, but can offer the necessary failure analysis information in order to understand and correct process or material problems. This destructive method, however, cannot be used on all assemblies. In the past years, as area-array packages have been taking over as a major SMD of choice, board assemblers have been using X-ray technology for non-destructive inspection. X-ray has proven its usefulness in the detection of typical problems such as voids, misalignments, opens and shorts. Additionally, this technology is continuing to increase its effectiveness, particularly from a magnification and resolution standpoint. Three factors, however, can make the use of this technology at times somewhat limiting: proper interpretation of the image data; the ability to "see" particular defects, such as delamination in the form of micro cracks; and the cost of the equipment. The topside ball delamination of lead-free FC and CSP solder joints can present difficulties for even the best 3D X-ray equipment.

ZUSAMMENFASSUNG

Mit dem derzeitigen Übergang zur bleifreien Herstellung von Baugruppen ergeben sich in den Unternehmen viele geänderte Anforderungen. Wie mittlerweile für Spezialisten hinlänglich bekannt sein dürfte, liegt die Löttemperatur (Liquidus) für bleifreie Pastenlegierungen um etwa 20 K höher als beim herkömmlichen, bleihaltigen Material. Das verengt erheblich das Prozessfenster, das definiert wird durch die zulässige Bauteiltemperatur einerseits und den Lot-Liquidus andererseits. Insbesondere bei den winzigen Löthöckern (Bumps), die unter Feld-Array-Packages verdeckt liegen (Flip-Chip, CSP, BGA usw.), muss man bei ungünstig gewählten Materialien mit unterschiedlichen Ausdehnungskoeffizienten nach dem Löten mit Defekten rechnen. Mit einer Spezialoptik kann man nun auch in diesem miniaturisierten Bereich von einem Punkt, der sich nur noch 0,015 mm (15 Mikron) über der Leiterplatte befindet, ein Bild zum oberen Teil solcher Komponenten aufnehmen und damit solche Fehler erkennen.

RÉSUMÉ

Le passage à la fabrication de sous-groupes sans plomb qui s'opère actuellement met les entreprises face à de nombreuses exigences modifiées. Ainsi que les spécialistes le savent bien aujourd'hui, la température de brasage (Liquidus) pour les alliages sans plomb est supérieure d'environ 20 K à celle des alliages conventionnels contenant du plomb. La fenêtre définie par la température admissible du composant d'une part et le point de fusion de la soudure de l'autre s'en trouve considérablement rétrécie. Dans le cas notamment des minuscules bumps (points de soudure) cachés sous les feld-array-packages (flip-chip, CSP, BGA, etc.), il faut s'attendre, si le choix des matières n'est pas optimal, à des coefficients de dilatation différents après le brasage et à des défauts. Grâce à une optique spéciale, malgré cette miniaturisation d'un point qui ne se trouve que 0,015 mm (15 microns) au-dessus de la carte imprimée, il est désormais possible de prendre une image du dessus des composants et de reconnaître de tels défauts.

SOMMARIO

Con l'attuale passaggio alla produzione senza piombo di aggregati, si presentano alle aziende numerosi e molteplici nuovi obiettivi. Come gli specialisti già sanno da lungo tempo, la temperatura di saldatura (Liquidus) per le paste di saldatura è di circa 20 K più elevata rispetto a quella dei materiali contenenti piombo. Ciò riduce notevolmente i tempi del processo, definiti dalla temperatura massima dei componenti da un lato e dal liquidus di saldatura dall'altro. Soprattutto per quanto concerne le microsfere di saldatura (Bumps) che restano coperte negli Array packages (Flip-Chip, CSP, BGA ecc.), nel caso siano stati scelti materiali con diversi coefficienti di dilatazione, bisogna considerare che dopo la saldatura è possibile che emergano dei difetti. Con una speciale tecnica ottica è possibile, anche in questo campo miniaturizzato, ottenere un'immagine della parte superiore di tali componenti da un punto ubicato a soli 0,015 mm (15 micron) sopra la piastra conduttrice e riconoscere tali errori.

Since its introduction to the market in 1999, manual BGA optical inspection equipment has become a state-of-the-art supplement to offline X-ray systems. Until now, however, its limitation lay in the fact that the optical system could inspect only the bottom side joint of low-profile packages such as micro BGAs, FCs and CSPs. In other words, the acute problem of topside ball delamination of FCs and CSPs could not be properly inspected by existing BGA-optical inspection gear. The introduction of a newly designed flip-chip optical inspection system now makes the visual verification of the critical defect area possible, and is a cost-effective alternative to destructive methods.

Low-profile CSPs and FCs will require the improved inspection capabilities of an optical head designed for visual inspection. The iris of the original BGA optical inspection system sits approximately 0.3mm from the surface of the PCB. This provides a "look-down image," as seen in figure 11, of a flip chip whose standoff or gap height is only 0.05mm. The flip-chip optical head has now lowered the iris to approximately 0.015mm. This means that it is now possible to "look up," as seen in figure 12, at even the topside of the flip-chip joint to avoid possible defects such as topside delamination. This critical topside fillet of FCs and CSPs was never before seen by any BGA optical inspection equipment on the market. Figure 12 reveals the importance of this optical innovation by discovering precisely the problem, topside delamination of a low-profile microBGA.

Figure 14: Interior topside fillet OK

Figure 15: Interior topside fillet deformed

Figure 16: Interior topside fillet OK

Figure 17: Interior topside fillet delaminated

Figure 18: Topside delamination visible

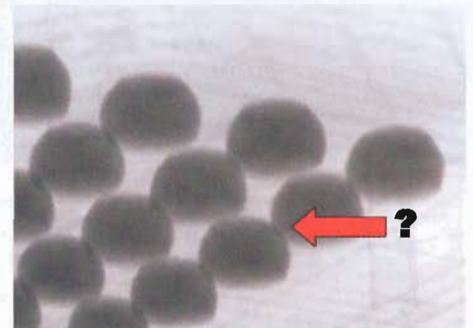

Figure 19: X-ray image of same defect very difficult to detect

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Toshio Nakamura and Gary Yu Gu: Mechanical Behaviors of Flip-Chip Packaging.

Gary Yu Gu and Toshio Nakamura: 3D Interfacial Delamination Near Solder Bumps in Flip-Chip Package.

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Based on the extremely low iris, the flip-chip optics even allows for the inspection of interior topside fillet problems in the middle of the component, as seen in figures 14 and 15, which were taken from the same microBGA.

The flip-chip optical inspection system has been successfully used to detect critical defects in a production line where lead-free CSPs are used. The topside fillets of a low-profile, lead-free CSP reveals that the middle ball in figure 16 has a proper topside fillet, whereas the left-side corner ball in figure 17 shows obvious delamination.

As mentioned before, X ray inspection is up-to-date and a necessary technology for the non-destructive inspection of assemblies. The particular defect of topside delamination, however, is very difficult or impossible to detect with X ray technology, as can be seen in the next images. Figure 18 was taken with the flip-chip optics, whereas figure 19 was taken with modern X-ray equipment.

It becomes obvious from these images that an X-ray system alone was not capable of discovering this topside delamination, which resulted for example in a 0.02mm micro crack on a lead-free microBGA. The use of such an optical inspection system which can compliment X-ray use, especially in a lead-free environment, should be considered as a sensible requirement.

Thorough procedure of first-article-inspection

The specific defect of component-side ball delamination of area-array packages, in particular FCs and CSPs, in the lead-free process puts higher challenges to the verification equipment. The existing problem of component-side delamination will be exacerbated in a lead-free process. With this knowledge, therefore, it is essential to implement proper inspection procedures to guarantee a quality lead-free FC and CSP soldering process. Failing to detect such fatal process defects will result in in-field failures, and will generate unnecessary warranty and repair costs. Board assemblers implementing lead free and using low-profile area-array packages should consider using appropriate optical inspection technologies designed to detect these defects in a non-destructive manner. The implementation of thorough first-article-inspection procedures with such equipment is a cost-effective alternative to the high costs of destructive methods, or the even higher costs of fatal defects being undetected. This can be seen as an opportunity to increase process quality and increase product reliability in the lead-free age.

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